PVP 14

Code: CS2T4

I B.Tech - II Semester – Regular/Supplementary Examinations
April - 2019

DIGITAL LOGIC DESIGN
(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) Reduce AB + (AC)' + AB'C (AB + C).

b) Determine the value of base 'X' if $(225)_X = (341)_8$.

c) Define don't care condition with an example.

d) Perform $(15)_{10}$ - $(28)_{10}$ using 2's complement representation.

e) Define fan-out of a logic gate.

f) Implement OR gate using NAND gates.

g) Define priority encoder.

h) Express function (xy+z)(y+xz) in sum of minterms and product of maxterms.

i) What are the applications of shift register?

j) Define PAL and PLA.

k) Show characteristic equation of JK-FF.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Convert each pair of decimal number to BCD and add
   i) $(65)_{10} + (58)_{10}$ ii) $(113)_{10} + (101)_{10}$ 8 M

   b) Using 10's complement, subtract
   i) $(72532)_{10} - (3250)_{10}$ ii) $(3250)_{10} - (72532)_{10}$
   What do you infer from the results? 8 M

3. Using K-map method determine the prime implicant and obtain the possible minimal expression for the following function
   $F(A,B,C,D) = \Sigma m(8,12,13) + d(1,2,4,6,7,11)$ 16 M

4. a) Design a BCD adder using 4-bit binary adders. 8 M

   b) Implement the following Boolean function using 8:1 MUX
   $F(P,Q,R,S)=\sum(0,1,3,4,8,9,15)$ 8 M

5. a) Illustrate the PLA implementation of the function
   $F(xl, x2, x3) = \Sigma m\ (1,2,4,7)$. 8 M

   b) Design a code converter circuit that converts Gray code to BCD using PAL. 8 M

6. Design a register to perform left shift and right shift for the following data 10110101. 16 M